TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
ITL.0513US

In Re Application Of: **Luke A. Johnson**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/752,125	December 29, 2000	Khai Tran	21906	2637	8725

Invention: **High-Speed Serial Data Recovery**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **May 26, 2005**

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Dated: **July 7, 2005**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Luke A. Johnson	Art Unit:	2637
Serial No.:	09/752,125	Examiner:	Khai Tran
Filed:	December 29, 2000	Atty Docket:	ITL.0513US P10388
For:	High-Speed Serial Data Recovery	Assignee:	Intel Corporation

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APPEAL BRIEF

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Cynthia L. Hayden

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-6, 8-13, 17-19, and 21-25 (Rejected).

Claims 7, 14-16, 18, 20, and 26-28 (Objected to).

Claims 1-28 are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. An apparatus (5, Fig. 1), comprising:

a storage device (240, Fig. 2) to store data (page 10, lines 2-6); and

a block (200, Fig. 2) to adjust the position of the data in the storage device (240) to account for the sampling rate of the apparatus (5) being different than the rate of the received data (page 11, lines 5-13).

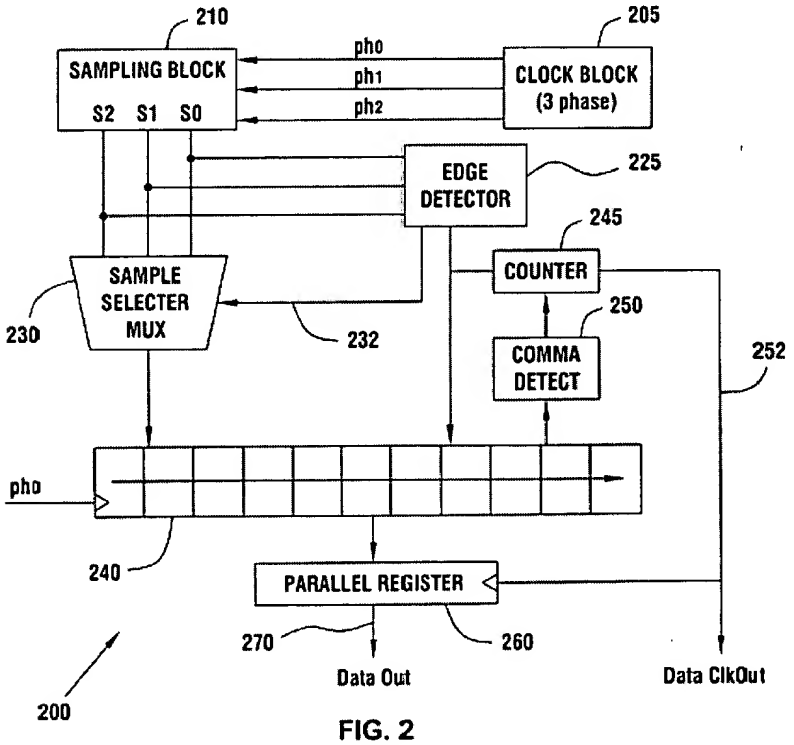

FIG. 2

10. An apparatus (5, Fig. 1), comprising:

a sampling block (210, Fig. 2) to sample incoming data using a plurality of sampling clocks (ph0, ph1, ph2) to provide a plurality of samples (page 7, lines 11-18);

a detector block (225, Fig. 2) to detect when the frequency of a sampling clock is different from the rate of the incoming data (page 9, lines 13-22); and

a storage device (240, Fig. 2) to adjust the position of the data in response to detecting the difference in frequency of the sampling clock and the incoming data (page 11, lines 5-13).

19. An apparatus (5, Fig. 1), comprising:

a clock block (215, Fig. 2) to generate a plurality of sampling clocks (page 7, lines 20-26);

a sampling block (210, Fig. 2) to sample data using the plurality of sampling clocks to generate a plurality of sample values (page 7, lines 11-18);

a detector block (225, Fig. 2) to detect that the frequency of a sampling clock is different from the frequency of the data being sampled (page 9, lines 13-22); and

a shift register (240, Fig. 2) to receive at least one of the plurality of sample values and to shift the at least one of the plurality of sample values in response to the difference in frequency between the sample clock and the sampled data (page 11, lines 5-13).

22. A method comprising:

storing data in a storage device (240, Fig. 2) (page 10, lines 2-6); and

adjusting the location of the data in the storage device (240) to account for a difference in the frequency of the sampling rate versus the data rate of the data being received in the storage (page 11, lines 5-13).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Are Claims 1-6, 8-13, 17-19, and 21-25 Unpatentable Over Nishimura in View of Byrne?

ARGUMENT

A. **Are Claims 1-6, 8-13, 17-19, and 21-25 Unpatentable Over Nishimura in View of Byrne?**

Claim 1 calls for a block to adjust the position of data in a storage device "to account for the sampling rate of the apparatus being different than the rate of the received data." In other words, the position of the data is adjusted, not just for any reason, but to account for the sampling rate of the apparatus being different.

It is conceded that Nishimura does not teach the sampling rate being different. See the first two lines of page 3 of the office action. This being so, Nishimura cannot teach adjusting the position of data to account for the sampling rate being different.

Nonetheless, it is observed that, in general, Nishimura teaches adjusting the position of data in the storage device. See the second to last line of page 2 of the office action. The claim calls for adjusting the position of the data to account, not just for anything, but only to account for the sampling rate of the apparatus being different than the rate of the received data. Since Nishimura does not even teach the sampling rate being different, he cannot teach adjusting position to account for the sampling rate difference.

The final office action observes, in the first full paragraph of page 3, that Byrne teaches sampling rates could be different. But, even if sampling rates are different, there is nothing that suggests changing the position of the data in the storage device to account for the sampling rate being different.

Therefore, a *prima facie* rejection of claim 1 is not made out and the rejection should be reversed. On the same basis, the rejection of claim 22 should be reversed.

Similarly, claim 10 calls for a storage device to adjust the position of data in response to detecting the different in frequency of the sampling clock and the incoming clock. No such operation is anywhere suggested in either reference or by any reasonable combination of the references suggested by the references themselves.

The only rationale to combine the references is that it would have been obvious "to detect the difference between the sampling rate of the incoming signal and the sampling clock" and to incorporate that into the teachings of Nishimura to compensate for oversampling. But, even if

one somehow deduced this rationale, it still does not teach changing the position of the data in response to the difference in frequency between the sample clock and the sampled data.

Therefore, the rejection of claim 10 should be reversed.

The rejection of claim 9 should be reversed.

* * *

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: July 7, 2005

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CLAIMS APPENDIX

The claims on appeal are:

1. An apparatus, comprising:

a storage device to store data; and

a block to adjust the position of the data in the storage device to account for the sampling rate of the apparatus being different than the rate of the received data.

2. The apparatus of claim 1, wherein the block adjusts a portion of the data in response to receiving a plurality of bits in response to sampling a portion of an incoming data.

3. The apparatus of claim 1, wherein the block comprises a detector to detect the at least one sampling error.

4. The apparatus of claim 3, comprising a counter block to provide a clock substantially synchronous with the data in response to detecting the at least one sampling error.

5. The apparatus of claim 1, wherein the block comprises a sampling block to sample incoming data using a plurality of sampling clocks to provide a plurality of samples.

6. The apparatus of claim 5, wherein the block comprises a multiplexer to receive the plurality of samples and provide a desirable sample to the storage device from the plurality of samples in response to a control signal.

7. The apparatus of claim 5, including a detector block to adjust the position of the data based on detecting at least one of a phase lag and a phase lead based on the plurality of samples.

8. The apparatus of claim 1, wherein the block does not shift the data in response to detecting duplicate sampling values of incoming data.

9. The apparatus of claim 1, wherein the storage device is a variable shift register.

10. An apparatus, comprising:

a sampling block to sample incoming data using a plurality of sampling clocks to provide a plurality of samples;

a detector block to detect when the frequency of a sampling clock is different from the rate of the incoming data; and

a storage device to adjust the position of the data in response to detecting the difference in frequency of the sampling clock and the incoming data.

11. The apparatus of claim 10, wherein the storage device is a shift register.

12. The apparatus of claim 11, wherein the storage device is a variable shift register.

13. The apparatus of claim 12, further comprising a counter block to count a number of shifts of the variable shift register.

14. The apparatus of claim 13, further comprising a comma detect block to reset the counter block in response to detecting a unique sequence of bits.

15. The apparatus of claim 13, wherein the counter block is one of a variable shift register and an adder circuit.

16. The apparatus of claim 13, wherein the detector is one of a phase detector and an edge detector.

17. The apparatus of claim 10, wherein the sampling block samples the incoming data using three sampling clocks to provide three samples.

18. The apparatus of claim 10, further comprising a multiplexer to receive the plurality of samples and provide desirable sample from the plurality of samples to the storage device based on a control signal from the detector block.

19. An apparatus, comprising:

a clock block to generate a plurality of sampling clocks;

a sampling block to sample data using the plurality of sampling clocks to generate a plurality of sample values;

a detector block to detect that the frequency of a sampling clock is different from the frequency of the data being sampled; and

a shift register to receive at least one of the plurality of sample values and to shift the at least one of the plurality of sample values in response to the difference in frequency between the sample clock and the sampled data.

20. The apparatus of claim 19, wherein the detector is an edge detector.

21. The apparatus of claim 19, wherein the shift register is a variable shift register.

22. A method comprising:

storing data in a storage device; and

adjusting the location of the data in the storage device to account for a difference in the frequency of the sampling rate versus the data rate of the data being received in the storage.

23. The method of claim 22, further comprising sampling incoming data to provide a plurality of samples.

24. The method of claim 23, further comprising detecting at least one sampling error in the plurality of samples.

25. The method of claim 24, further selecting a desirable sample from the plurality of samples and storing the desirable sample in the storage device.

26. The method of claim 22, wherein sampling the incoming data comprises sampling the incoming data at a rate at least three times faster than the rate of the incoming data.

27. The method of claim 22, wherein adjusting the location comprises shifting the data by two location in the storage device to account for sampling frequency being slower than a rate of an incoming data.

28. The apparatus of claim 22, wherein adjusting the location comprises not shifting the data in the storage device to account for sampling frequency being faster than a rate of an incoming data.